WHAT	IS	CL	AIN	ИED	IS:

	WHAT IS CLAIMED IS:				
1	A shares num singuit samunising				
1	1. A charge pump circuit/comprising:				
2		a first transistor;			
3	a first capacitor coupled to the first transistor;				
4	a second transistor coupled to the first transistor; and				
5	a second capacitor coupled to the second transistor, wherein the second				
6	transistor has a lower threshold voltage than the first transistor at a common source voltage				
1	2. The charge pump circuit of claim 1 further comprising:				
2	a third transistor coupled to the second transistor; and				
3	a third capacitor coupled to the third transistor, wherein the third transistor ha	ıS			
	a lower threshold voltage than the first transistor at a common source voltage.				
]]	3. The charge pump circuit of claim 2 further comprising:				
2	a fourth transistor coupled to the third transistor; and				
3	a fourth capacitor coupled to the fourth transistor, wherein the fourth transistor	r			
4	has a lower threshold voltage than the first transistor at a common source voltage.				
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]	4. The charge pump circuit of claim 3 further comprising:				
2	a fifth fransistor coupled to the fourth transistor; and				
3	a fifth capacitor coupled to the fifth transistor, wherein the fifth transistor has	a			
4	lower threshold voltage than the first transistor at a common source voltage.				
1	5. The charge pump circuit of claim 3 further comprising four diode-				
2	connected transistors, wherein each diode-connection transistor is coupled to a gate of one of	f			
3	the first, second, third, and fourth transistors.				
1	6. The charge pump circuit of claim 4 further comprising:				
2	a sixth transistor coupled to the fifth transistor;				
3	a sixth capacitor coupled to the sixth transistor;				
4	a seventh transistor coupled to the sixth transistor;				
5	a seventh capacitor coupled to the seventh transistor;				
6	an eighth transistor coupled to the seventh transistor; and				
7	an eighth capacitor coupled to the eighth transistor, wherein the sixth, seventh	ı,			
8	and eighth transistors each have a lower threshold voltages than the first transistor at a				
9	common source voltage.				

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and

7.	The charge pump circuit of claim 6 further comprising:
a ninth	transistor coupled to the eighth transistor;
a ninth	capacitor coupled to the ninth transistor
a tenth	transistor coupled to the ninth transistor;
a tenth	capacitor coupled to the tenth transistor;
an elev	venth transistor coupled to the tenth transistor; and
an elev	venth capacitor coupled to the eleventh transistor, wherein the ninth,
venth tra	ansistors each have a lower threshold voltages than the first transistor at
irce vol	tage.
	The charge pump circuit of claim further comprising:
a twelf	th transistor coupled to the eleventh transistor;
a twelf	th capacitor coupled to the twelfth transistor;
a thirte	enth transistor coupled to the twelfth transistor;
a thirte	enth capacitor coupled to the hirteenth transistor, wherein the twelfth
transist	ors each have a lower threshold voltages than the first transistor at a
ce volta	ge.
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	The charge pump circuit of claim 8 further comprising:
	eenth transistor coupled to the thirteenth transistor;
a fourt	eenth capacitor coupled to the fourteenth transistor;
a fiftee	enth transistor coupled to the fourteenth transistor; and
an fifte	eenth capacitor coupled to the fifteenth transistor, wherein the fourteenth
ransisto	rs each have a lower threshold voltages than the first transistor at a
ce volta	ge.
10.	The charge pump circuit of claim 3 wherein the first and third
coupled	to receive a first clock signal, and the second and fourth capacitors are
eive a s	econd clock signal.
11.	The charge pump circuit of claim 10 further comprising:
a fifth	capacitor coupled to the first transistor and a third clock signal;
a sixth	capacitor coupled to the second transistor and a fourth clock signal;
a sever	nth capacitor coupled to the third transistor and the third clock signal;
	a ninth a ninth a ninth a tenth a tenth an elev venth tra urce vol 8. a twelf a thirte transist ce volta 9. a fourt a fourt a fiftee an fiftee transisto ce volta 10. coupled eive a se 11. a fifth a sixth

6		an eighth capacitor coupled to the fourth transistor and the fourth clock sign
1		12. A method for receiving an input voltage and providing a/boosted
2	output voltage	e, the method comprising:
3		increasing a first voltage at a first capacitor;
4		coupling the first capacitor to a second capacitor through a first transistor;
5		increasing a second voltage at the second capacitor; and
6		coupling the second capacitor to a third capacitor through a second depletion
7	transistor.	
1		13. The method of claim 12 further comprising/
2		increasing a third voltage at the third capacitor;
3		coupling the third capacitor to a fourth capacitor through a third depletion
	transistor;	
5		increasing a fourth voltage at the fourth capacitor; and
<u></u>		coupling the fourth capacitor to a fifth capacitor through a fourth deletion
7	transistor.	
		14. The method of claim 13 further comprising:
i o		increasing a fifth voltage at the fifth capacitor;
Š		coupling the fifth capacitor to a sixth capacitor through a fifth depletion
10 4	transistor;	coupling the first capacitor to a given capacitor through a first depiction
5	trunsistor,	increasing a sixth voltage at the sixth capacitor; and
6		coupling the sixth capacitor to a seventh capacitor through a sixth depletion
7	transistor.	
1		15. The method of claim 14 further comprising:
2		increasing a seventh voltage at the seventh capacitor;
3		coupling the seventh capacitor to a eighth capacitor through a seventh
4	depletion tran	sistor;
5		increasing an/eighth voltage at the eighth capacitor; and
6		coupling the eighth capacitor to a ninth capacitor through a eighth depletion
7	transistor.	
1		16. The method of claim 15 further comprising:
2		increasing a ninth voltage at the ninth capacitor:

3		coupling the ninth capacitor to a tenth capacitor through a ninth depletion		
4	transistor;			
5		increasing a tenth voltage at the tenth capacitor; and		
6		coupling the tenth capacitor to an eleventh capacitor through a tenth depletion		
7	transistor.			
.1		17. The method of claim 16 further comprising:		
2		increasing an eleventh voltage at the eleventh capacitor;		
1^3		coupling the eleventh capacitor to a twelfth capacitor through an eleventh		
(4	depletion tran	sistor;		
5		increasing a twelfth voltage at the twelfth capacitor; and		
6		coupling the twelfth capacitof to a thirteenth capacitor through a twelfth		
	depletion tran	sistor.		
u =		The most had a fall of 14 when in the first transition has a supply		
d	4111-4	18. The method of claim 14 wherein the first transistor has a greater		
12		age than the second, third, fourth, fifth and sixth transistors at a common source		
	voltage.			
<u> </u>		19. The method of claim 13 further comprising:		
-[2		providing a first clock signal to the first and third capacitors; and		
		providing a second glock signal to the second and the fourth capacitors.		
1		20. The method of claim 19 further comprising:		
2		coupling a gate and a drain/source of the first transistor through a fifth		
3	transistor in re	esponse to the first clock signal;		
4		providing a third clock signal to fifth and sixth capacitors coupled to gates of		
5	the first and th	nird transistors;		
6		coupling a gate and a drain/source of the second transistor through a sixth		
7	transistor in re	sistor in response to the second clock signal;		
8		providing a fourth clock signals to sixth and seventh capacitors coupled to		
9	gates of the se	econd and fourth transistors; and		
10		coupling a gate and a drain/source of the third transistor through a seventh		
11	transistor in re	esponse to the first clock signal.		
1		21. A charge pump circuit comprising:		
2		a first stage comprising a first depletion field-effect transistor;		

3	a second stage comprising a second depletion field-effect transistor, the			
4	cond stage being coupled to the first stage;			
5	a first capacitor coupled to the first stage; and			
6	a second capacitor coupled to the second stage.			
1	22. The charge pump circuit of claim 21 further comprising:			
2	a third stage comprising a third depletion field-effect transistor, the third stage			
3	being coupled to the second stage;			
4	a fourth stage comprising a fourth depletion field-effect transistor, the fourth			
5	stage being coupled to the third stage;			
6	a third capacitor coupled to the third stage; and			
	a fourth capacitor coupled to the fourth stage.			
	23. The charge pump circuit of claim 22 further comprising:			
_ 2	a fifth stage comprising a fifth depletion field-effect transistor, the fifth stage			
⊒3	being coupled to the fourth stage;			
4	a sixth stage comprising a sixth depletion field-effect transistor, the sixth stage			
<u></u> 5	being coupled to the fourth stage;			
= 6	a fifth capacitor coupled to the fifth stage; and			
≓6 □7 □	a sixth capacitor coupled to the sixth stage.			
1	24. The charge pump circuit of claim 23 further comprising:			
2	a seventh stage comprising a seventh depletion field-effect transistor, the			
3	seventh stage being coupled to the sixth stage;			
4	an eighth stage comprising an eighth depletion field-effect transistor, the			
5	eighth stage being coupled to the seventh stage;			
6	a seventh capacitor coupled to the seventh stage; and			
7	an eighth capacitor coupled to the eighth stage.			
1	The charge pump circuit of claim 24 further comprising:			
2	a ninth stage comprising a ninth field-effect transistor, the ninth stage being			
3	coupled to the eighth stage;			
4	a tenth stage comprising a tenth depletion field-effect transistor, the tenth stage			
5	being coupled to the ninth stage;			



6	an eleventh stage comprising an eleventh field-effect transistor, the eleventh
7	stage being coupled to the tenth stage;
8	a ninth capacitor coupled to the ninth stage;
9	a tenth capacitor coupled to the tenth stage; and
10	an eleventh capacitor coupled to the eleventh stage.
1	26. The charge pump circuit of plaim 22 wherein the first and third
2	capacitors are coupled to receive a first clock signal, and the second and fourth capacitors are
3	coupled to receive a second clock signal.
1	27. The charge pump circuit of claim 26 further comprising:
2	a fifth capacitor coupled to a gate of the first depletion transistor;
3	a sixth capacitor coupled to a gate of the second depletion transistor;
4	a seventh capacitor coupled to a gate of the third depletion transistor; and
3	an eighth capacitor coupled to a gate of the fourth depletion transistor, wherein
6	the fifth and seventh capacitors are coupled to receive a third clock signal, and the sixth and
7	eighth transistors are coupled to receive a fourth clock signal.
-T	28. The charge pump circuit of claim 27 further comprising:
<u> </u>	a fifth transistor coupled across two terminals of the first transistor and to the
אל ה	first capacitor;
	a sixth transistor coupled across two terminals of the second transistor and to
5	the second capacitor;
6	a seventh transistor coupled across two terminals of the third transistor and to
7	the third capacitor; and
8	an eighth transistor coupled across two terminals of the fourth transistor and to
9	the fourth capacitor.
1	29. An integrated circuit comprising:
2	programmable logic circuitry; and
3	a charge pump circuit comprising:
4	first and second stages coupled together,
5	a first capacitor coupled to the first stage, and
6	a second capacitor coupled to the second stage, wherein the second
7	stage comprising a depletion transistor.